

PowerPC 440GX

Embedded Processor



With speeds of up to 800 MHz, the PowerPC 440GX processor offers the versatility and bandwidth required for demanding networking and storage applications. This highly integrated device supports PCI-X bus devices and DDR333 memory. With embedded state-of-the-art peripheral cores, the 440GX processor is ideal for networking control plane applications, RAID controllers, iSCSI processing, and storage area networking (SAN) equipment.

Benefits

- Delivers 533 MHz to 800 MHz performance (CPU)
- Provides 256-Kbyte on-chip SRAM, configurable as an L2 cache or as packet/code-store memory for low-latency access
- Integrates state-of-the-art peripherals, such as PCI-X and DDR SDRAM
- Four Ethernet interfaces, including two 10/100/1-Gbit MACs, for increased bandwidth and connectivity
- Embeds TCP/IP Acceleration Hardware (TAH), freeing CPU core cycles for other demands
- Messaging unit facilitates PCI communications for increased application performance
- PowerPC application code compatibility
- Processor parity for enhanced data integrity
- Low power dissipation and small form factor for high-density and power-conscious applications.

The PowerPC 440 Core

To enhance overall throughput, the PowerPC 440 superscalar core incorporates a 7-stage pipeline and executes up to two instructions per cycle. Its large 32-Kbyte data cache and 32-Kbyte instruction cache are 64-way set-associative. Versatile configurations enhance performance tuning while optional parity protection preserves data integrity. For additional system performance, the PowerPC 440 core includes dynamic branch prediction and 24 digital signal processing (DSP) instructions, as well as non-blocking caches that can be managed in either write-through or write-back mode.

Bus Architecture

The PowerPC 440GX processor is designed with three on-chip buses: a processor local bus (PLB), an on-chip peripheral bus (OPB), and a device control register bus (DCR). The processor core, memory controller, and PCI-X bridge connect through the high-bandwidth PLB. The PLB supports speeds up to 166 MHz, and offers separate read and write data buses, while its 36-bit address path offers 64 Gbytes of memory addressability. To maximize on-chip resource utilization, the 440GX offers performance tuning thanks to its integrated PLB performance monitor. Less demanding I/O devices are served by the 32-bit OPB.

Flexible Memory Configurations

256 Kbytes of on-chip SRAM can be configured either as a performance-enhancing L2 cache, or as memory-mapped SRAM for low-latency access. Used as L2, the 256-Kbyte SRAM is a 4-way set-associative, unified data/instruction cache, which can benefit many applications. As memory-mapped SRAM, it has lower memory access latency than the SDRAM, offering quick access to crucial code or data. Software-controlled and with parity support, this memory is ideal for storing data packets, critical code segments, Ethernet or DMA descriptors, or other application-specific data. When configured as a memory-mapped region, this SRAM is accessible from any PLB master, which can further improve application performance.

An on-chip double data rate (DDR) SDRAM controller supports up to DDR333 memory, for a sustainable peak bandwidth 2.6-Gbyte/s. 8-bit ECC protection is also available.

PCI Interface

PowerPC 440GX's PCI-X interface supports 32- or 64-bit PCI-X v1.0 devices at frequencies of up to 133 MHz, for 800 Mbytes/s of sustained bandwidth and 1.1 Gbytes/s of peak bandwidth. An I2O spec messaging unit facilitates communication between the PCI-X bus and the 440GX core for even greater efficiency. For enhanced manageability and functionality, the 440GX can be booted from the PCI-X bus memory.

Gigabit Ethernet and TCP/IP Assist

For increased bandwidth and connectivity, the 440GX offers four on-chip Ethernet interfaces, including two 10/100/1-Gbit MACs with jumbo frame support. The two 10/100/1000 ports are supported by the chip's embedded TCP/IP acceleration hardware (TAH), freeing CPU core cycles for other application demands

External Bus Interface

To accommodate connectivity with other devices, the PowerPC 440GX offers a 32-bit bus supporting up to eight ROM, RAM or slave peripheral I/O devices and speeds up to 83 MHz. 4-Channel DMA and external bus mastering and also supported.

Standard Peripherals

The PowerPC 440GX offers two serial ports (16750 compatible UART), support for up to 32 general-purpose I/O (GPIO) and two Phillips IIC spec compatible IIC controllers. A JTAG interface is also provided for debugging purposes.

PowerPC Partners Ecosystem

AMCC's embedded PowerPC processors are supported by an extensive ecosystem of products and services from a wide range of leading suppliers. AMCC's PowerPC Partners program includes industry-standard providers of:

- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training

For full details of the products and services available through the PowerPC Partners program, or to browse support available for a specific processor, visit:

<http://www.amcc.com/Embedded/Partners>

PowerPC 440GX

AMCC also provides an evaluation kit for this PowerPC processor, including an optimized evaluation board as well as sample applications and other software.

Features

- Speed (frequency): 533 MHz to 800 MHz
- Performance: 2.0 DMIPS/MHz (1,600 DMIPS @ 800 MHz)
- Memory management unit with parity
- Up to 166 MHz CoreConnect Processor Local Bus (128-bit PLB) with separate read and write databases
- Up to 83 MHz CoreConnect on-chip peripheral bus (32-bit OPB)
- 36-bit address, 64-Gbyte memory map
- 32/64-bit DDR200-DDR333 SDRAM controller
- Up to four 512-Mbyte logical banks, for a total of 2 Gbytes memory
- Optional 8-bit ECC protection
- Sustainable 2.6-Gbyte/s peak bandwidth at DDR333
- 32/64-bit PCI-X Interface, up to 133 MHz with 800-Mbyte/s sustained bandwidth and up to 1.1-Gbyte/s peak bandwidth
- Support for PCI v2.3, up to 66 MHz
- I2O specification Messaging unit
- 256-Kbyte on-chip SRAM configurable as either L2 cache or packet/code store memory
- Parity support on SRAM
- Unified, 4-way set-associative L2 cache
- Up to 83 MHz, 32-bit address bus, 32-bit data bus External Bus Control (EBC) Interface
- Support for up to 8 ROM, RAM, or slave peripheral I/O devices
- 4-channel DMA support for external peripherals
- External bus master controller for access to internal peripherals
- Support for memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers
- Scatter/gather capability
- 128-byte buffer with programmable thresholds
- Up to four Ethernet ports, including two 10/100/1-Gbit Ethernet ports with jumbo frame support and TCP/IP assist, configurable as 2 SMII, 2 RGMII/RTBI, or 1 GMII/TBI interface
- TCP/IP acceleration hardware (TAH) available on the two 10/100/1-Gbit Ethernet ports
- Two serial ports, one 9-pin and one 5-pin
- Two IIC controllers, designed to Phillips IIC specification
- Up to 32 GPIO – Up to 18 external interrupts
- Support for JTAG board testing, JTAG debuggers, and 4xx instruction trace interface
- Available in ceramic packages (non RoHS- and RoHS-compliant versions) and plastic packages (non RoHS- and RoHS-compliant versions)

For more information, please visit <http://www.amcc.com>.

Specifications

Technology

- 0.13 μ m CMOS

Performance (estimated)

- 1,600 DMIPS @ 800 MHz

Frequency

- CPU: 533 MHz to 800 MHz
- Memory:
 - 32-bit width: 800 Bytes/s (DDR200) to 1.3 Gbytes/s (DDR333)
 - 64-bit width: 1.6 Bytes/s (DDR200) to 2.6 Gbytes/s (DDR333)
- PCI: 33 MHz to 66 MHz
- PCI-X: 50 MHz to 133 MHz

Typical Power Dissipation

- 4 W @ 533 MHz (application dependent)

Case Temperature Range

- -40° C to +85° C extended temperature range (-40 to +105° C) available at 533 MHz

Power Supply

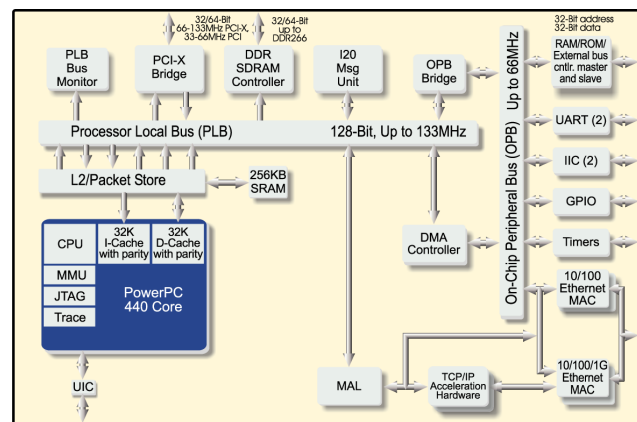
- 1.5 V, 2.5 V, or 3.3 V depending on interface

Signal I/Os

- 406

Packaging

- 552-ball, 25 mm x 25 mm CBGA (with 1.0-mm pad pitch)
- 552-ball, 25 mm x 25 mm FC-PBGA (with 1.0-mm pad pitch)



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